Page 1 of 1 Form PTO-1449 (modified) Atty. Docket No. Serial No. 2000.038800/TT3761 09/870,889 List of Patents and Publications for Applicant's Applicant Weber et al. INFORMATION DISCLOSURE STATEMENT Filing Date: Group: (Use several sheets if necessary) May 10, 2001 2131 U.S. Patent Documents **Foreign Patent Documents** Other Art See Page 1 See Page 1 See Page 1 **U.S. Patent Documents** Exam. Ref. **Document** Date Name Class Sub Filing Date of Init. Des. Number Class App. Al RECEIVED **A2** A3 OCT 1 0 2002 A4 OFFICE OF PETITIONS **A5 Foreign Patent Documents** Exam. Ref. **Document Date** Country Class Sub **Translation** Number Yes/No Init. Des. Class Bl B2 **B3** Technology Center 2100 **B5** Other Art (Including Author, Title, Date Pertinent Pages, Etc.) Exam. Ref. Citation Init. Des. Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97) CI C2 Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99) C3 FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994) C4 Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000) C5 "Handbook of Applied Cryptography" CRC Press 1997 pp. 154 - 157, 160 - 161, 191 - 198, M()203 - 212

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